

CLAIMS

What is claimed is:

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1 1. A method comprising:
2 enabling a special programming mode of a memory by entering a special
3 programming access code in a state controller, wherein the memory includes
4 automation circuitry for program verification and wherein the special
5 programming mode disables internal program verification by the memory;
6 programming a plurality of words into the memory without the memory
7 performing internal program verification; and
8 exiting the special programming mode of the memory.

1 2. The method of Claim 1, further comprising verifying the plurality of
2 words programmed into the memory with a verification processor by resending
3 the plurality of words previously sent into the memory.

1 3. The method of Claim 2, wherein the verification processor is an
2 external host processor.

1 4. The method of Claim 2, further comprising enabling internal
2 program verification by the memory and wherein the verification processor
3 is (the memory internal program verification processor).

1 5. The method of Claim 2, wherein verifying further includes:
2 determining if all of the words in the plurality of words are verified;
3 if any one of the plurality of words does not verify, then repeat the
4 programming of the entire plurality of words and repeat the verification; and

5 if all of the plurality of words verify, then exiting the special programming
6 mode of the memory.

1 6. The method of Claim 2, wherein verifying further includes:
2 determining if all of the words in the plurality of words are verified;
3 if any one of the plurality of words does not verify, then repeat the
4 programming of the one word that did not verify and repeat the verification; and
5 if all of the plurality of words verify, then exiting the special programming
6 mode of the memory.

1 7. The method of Claim 1, wherein exiting the special programming
2 mode of the memory permanently disables the special programming user
3 interface.

1 8. The method of Claim 1, wherein exiting the special programming
2 mode of the memory enables internal program verification by the memory.

1 9. The method of Claim 1, wherein programming the plurality of words
2 into the memory further comprises using only a single programming pulse for
3 each bit of each word of the plurality of words.

1 10. The method of Claim 1, wherein the programming the plurality of
2 words into the memory without the memory performing internal program
3 verification continues until a programming ending condition is met.

1 11. The method of Claim 10, wherein the programming ending
2 condition is a pre-selected time.

4 a second memory coupled to the host processor; and
5 circuitry for comparing the plurality of words stored in the second
6 memory with a plurality of words read from the memory by the host
7 processor.

1 18. The apparatus of Claim 17, further including:
2 a circuit to reprogram the entire plurality of words if any one of the plurality
3 of words does not verify.

1 19. The apparatus of Claim 17, further including:
2 a circuit one word that did not verify.

1 20. The apparatus of Claim 13, wherein the circuit to exit the special
2 programming mode of the memory disables the special programming mode
3 circuitry.

1 21. The apparatus of Claim 13, wherein the circuit to exit the special
2 programming mode of the memory enables internal program verification by the
3 memory.

1 22. The apparatus of Claim 13, wherein the special programming mode
2 circuitry is disabled when a programming ending condition is met.

1 23. The apparatus of Claim 22, wherein the programming ending
2 condition is a pre-selected time.

1 24. The apparatus of Claim 22, wherein the programming ending
2 condition is an ending address.